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Low-power analog-to-digital conversion

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1 Abstract

The subject of this graduation project is low-power analog-to-digital conversion. A motivation for the subject is that power consumption is a critical criterion for some ADC applications. The first project goal is the investigation of low-power ADC architectures and building blocks on the conceptual and circuit level. The second project goal is the development of a chip to test and demonstrate some of these circuits.

Limitations on low-power analog-to-digital conversion are explored. It is concluded that the figure of merit, a widely accepted benchmark for low-power analog-to-digital conversion, does not correspond to fundamental limitations. It is also concluded that it depends on the number of bits how easy it is to reach a certain FOM.

The scope of an ADC is explored. Various conceptions exist about when a circuit deserves to be called ADC. A set of conditions is selected.

Various ADC architectures are qualitatively compared on their suitability for low-power analog-to-digital conversion. It is concluded that logarithmic approximation is the most suitable one for low-power analog-to-digital conversion. One such architecture is selected for development, the successive approximation architecture.

Building blocks for low-power analog-to-digital conversion are explored. These include techniques to dissipate less total comparator energy regardless of the comparator architecture. Level creation based on charge redistribution is explored and it is concluded that there is no fundamental lower limit on energy dissipation of digital-to-analog conversion. Also a new comparator architecture is developed that is efficient in terms of noise per energy.

A test and demonstration chip is developed using a 65nm process. According to post layout simulations it obtains a figure of merit of 4.6 fJ / conversion-step, which is about 35 times lower than the lowest value currently published.

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2 Introduction

An analog-to-digital converter (ADC) is one of the most common building blocks of modern integrated circuits. Many different designs are in use today to meet a very wide range of requirements. For some applications the power consumption of the ADC is a critical criterion.

The subject of this graduation project is low-power analog-to-digital conversion. The first project goal is the investigation of low-power ADC architectures and building blocks on the conceptual and circuit level. The second project goal is the development of a chip to test and demonstrate some of these circuits.

Chapter 3 explores limitations on low-power analog-to-digital conversion. Because an ADC is a signal processing building block signals are discussed first. Next signal processing and limitations on signal processing are discussed. These limitations include technology limitations and noise.

The purpose of a signal is conveying information. Properties of information are discussed next. Finally chapter 3 discusses some properties of analog-to-digital conversion. A figure of merit is discussed and compared to signal processing limitations.

Chapter 4 explores the scope of an ADC. Especially when developing a low-power ADC it is necessary to consider when a circuit can reasonably be called an ADC.

Various ADC architectures exist. In chapter 5 they are qualitatively compared on their suitability for low-power analog-to-digital conversion. A conclusion is drawn after considering the same aspects for every architecture.

In chapter 6 building blocks for low-power analog-to-digital conversion are explored. They are mainly geared towards logarithmic approximation with the main emphasis on successive approximation. First techniques are discussed to dissipate less total comparator energy regardless of the comparator architecture. Next level creation based on charge redistribution is discussed. After that work on a new comparator architecture is discussed.

Chapter 7 discusses the development of the test and demonstration chip. A 65nm process is used. Its specifications are chosen such that they are favorable for a low figure of merit.

In chapter 8 it is discussed which conclusions can be drawn from this project. It also contains some recommendations for future work.

3 Limitations on low-power analog-to-digital conversion

An ADC is a signal processing circuit. This chapter discusses some background on signal processing and various limitations. The reader should feel free to initially skip any part that seems familiar.

3.1 Signals and their electrical representation

This paragraph first discusses signals. Then electrical quantities are discussed. Next it is discussed how signals can be mapped onto electrical quantities. Finally working with signals is discussed.

3.1.1 Signals

A signal is something that can be used to convey information. It can be discrete or continuous in time and amplitude. An analog signal is continuous in both time and amplitude. A digital signal is discrete in both time and amplitude.

3.1.2 Electrical quantities

In an integrated circuit electrical quantities can be used to represent signals. The fundamental electrical quantities are charge and flux, which are manifested as voltages on capacitances and currents through inductors. Electrical quantities are usually considered to be time and amplitude continuous in nature.

3.1.3 Mapping of signals onto electrical quantities

An analog signal can straightforwardly be mapped onto an electrical quantity, because both are continuous. It is less straightforward to represent digital signals by electrical quantities. It is common practice to represent a bit by a node voltage. A digital one can be a voltage close to the positive supply voltage and a digital zero a voltage close to the negative supply voltage.

3.1.4 Working with signals

When considering an integrated circuit it is not feasible to take all known fundamental quantities and effects into account. Simplification is necessary in order to work with signals. The simplification an analog developer usually uses is to consider voltages as the main carrier of signals.

A circuit simulator has a numerical processing power that is superior to that of an analog developer. As a result less simplification is required and more state variables than just voltages can be taken into account. State variables can include for example charge, current and temperature. In principle a circuit simulator is just as suitable for an ADC with a voltage input as for an ADC with a different input. In a practical simulation environment not all state variables are available outputs by default.

3.2 Analog and amplitude-continuous time-discrete signal processing

Analog signals and amplitude-continuous time-discrete signals are both amplitude-continuous. Processing always reduces their signal integrity. The underlying mechanisms are mostly the same for both classes. Therefore these are discussed in the same section. First the class of amplitude-continuous time-discrete signals is discussed in paragraph 3.2.1. Next technology limitations and noise will be discussed.

3.2.1 Amplitude-continuous time-discrete signals

Amplitude-continuous time-discrete signals can arise from sampling analog signals. Sampling is often a first step in analog-to-digital conversion. Sampling is also required for switched capacitor filters. These filters can have implementation advantages over continuous-time filters.

The electrical quantities used to represent time-discrete signals can not truly be time-discrete. When, for example, a voltage has been sampled onto a capacitor there are still mechanisms causing deviations in the charge. These mechanisms can include current through an off resistance of a switch or electron tunneling through a MOST gate.

3.2.2 Technology limitations

In a bulk process, devices are manufactured with limited accuracy. As a results there are unknown lattice defects and there is uncertainty in doping and device dimensions. For a circuit designer the limited accuracy is manifested by device parameter variation, flicker noise and a minimum allowed feature size. Some fundamental limitation for these factors exists. So far, a newer and better controlled technology can give better results.

Device parameter variation is stochastic with a high correlation between devices on the same integrated circuit. Flicker noise is stochastic with a high correlation in time. The results of both effects on system behavior depends on design.

For hand calculations first-order models exist for the stochastic mismatch between components. Examples are the threshold voltage mismatch between equally designed transistors (1) and the capacitance mismatch between equally designed capacitors (2). A design manual can contain these matching parameters in some form. Compact models for simulation can contain a more complex model.

$$\sigma_{VT}=\frac{A_{VT}}{\sqrt{W\cdot L}}[V] \tag{1}$$

$$\sigma_C=A_C\cdot\sqrt{C}[F] \quad \Leftrightarrow \quad \frac{\sigma_C}{C}=\frac{A_C}{\sqrt{C}}\cdot 100[\%] \tag{2}$$

With careful layout a very large range of capacitor values obeying formula (2) can be made available. A process provider can specify a predefined capacitor layout for a limited capacitance range. The parameter A_C and minimum and maximum values for the capacitance are guaranteed. Custom layout is required when the provided capacitance range is insufficient for a purpose. The parameter A_C and minimum and maximum values can not be obtained from the design manual.

3.2.3 Noise

Thermal noise and shot noise result in relevant fundamental limitations for signal processing. Both are modeled by a Gaussian distribution with zero mean. In the time-domain they can be characterized by a standard deviation in an electrical quantity. Frequency-domain equivalents exist. Depending on the application noise can be regarded as time-continuous or time-discrete.

Thermal noise voltages and currents are best defined for a resistor (3). Similar formulas exist for a MOST. A theoretical gate-referred error voltage of a MOST in strong inversion is given by (4). The noise excess factor γ is close to one. In weak inversion it is shot noise and given by (5). Formula (6) is approximately valid for a MOST in weak inversion, with the parameter m close to two. Combining (5) and (6) gives (7).

$$\sigma_v = \sqrt{4 \cdot k \cdot T \cdot R \cdot B}[V] \quad \Leftrightarrow \quad \sigma_i = \sqrt{\frac{4 \cdot k \cdot T}{R} \cdot B}[A] \tag{3}$$

$$\sigma_v = \sqrt{\gamma \cdot \frac{4 \cdot k \cdot T}{gm} \cdot B} \approx \sqrt{\frac{4 \cdot k \cdot T}{gm} \cdot B}[V] \tag{4}$$

$$\sigma_v = \sqrt{2 \cdot q \cdot I_{DS} \cdot B} \cdot \frac{1}{gm}[V] \tag{5}$$

$$\frac{I_{DS}}{gm} \approx m \cdot V_{th} = \frac{m \cdot k \cdot T}{q}[V] \tag{6}$$

$$\sigma_v = \sqrt{2 \cdot q \cdot I_{DS} \cdot B} \cdot \frac{1}{gm} = \sqrt{2 \cdot q \cdot \frac{m \cdot k \cdot T}{q} \cdot \frac{1}{gm} \cdot B} = \sqrt{\frac{2 \cdot m \cdot k \cdot T}{gm} \cdot B} \approx \sqrt{\frac{4 \cdot k \cdot T}{gm} \cdot B}[V] \tag{7}$$

A time-discrete voltage signal can be obtained by sampling a time-continuous voltage signal onto a capacitor. The corresponding noise voltage is time-discrete as well. Its magnitude depends on the capacitance and is given in formula (8). The formula is valid after the transitional sampling effects and assumes sampling through a resistor with temperature T.

$$\sigma_v = \sqrt{\frac{k \cdot T}{C}}[V] \tag{8}$$

3.2.4 Power, energy and signal to noise ratio

Sometimes an electrical quantity can be associated with a resistor, capacitor or inductor. A corresponding power (9) or energy (10) can be calculated from magnitude. Formula (9) describes the power dissipated in a resistor. It can especially be useful for power calculations on time-continuous signal processing.

Formula (10) describes energy that is stored. It can especially be useful for power calculations on time-discrete signal processing. Capacitors in corresponding circuits are charged and discharged every cycle. During charging and discharging the stored energy is generally dissipated. Power dissipation is the product of the energy dissipation during one cycle and the cycle rate (11).

$$P = \frac{V^2}{R}[W] \quad \Leftrightarrow \quad P = I^2 \cdot R[W] \tag{9}$$

$$E = \frac{1}{2} \cdot C \cdot V^2[J] \quad ; \quad E = \frac{1}{2} \cdot L \cdot I^2[J] \tag{10}$$

$$P = E \cdot f[W] \tag{11}$$

Noise has a standard deviation that is often deterministic, paragraph 3.2.3. As a result noise powers and energies can be calculated using the same formulas. A signal to noise ratio (SNR) is the ratio of a signal power and a noise power or a signal energy and a noise energy. In formula (12) it is shown that the power ratio does not depend on an actual resistor value. Similarly the energy ratio does not depend on an actual capacitor or inductor value. Possible noise contributions from the components used to calculate the SNR have not been included in this consideration.

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{V^2/R}{\sigma_V^2/R} = \frac{V^2}{\sigma_V^2}[] \quad ; \quad SNR = \frac{P_{signal}}{P_{noise}} = \frac{I^2 \cdot R}{\sigma_I^2 \cdot R} = \frac{I^2}{\sigma_I^2}[] \tag{12}$$

For time-continuous signals the noise magnitude depends on the bandwidth. Formula (13) is a general expression where N_0 is the power spectral density.

$$SNR = \frac{P}{N_0 \cdot B}[] \tag{13}$$

3.2.5 Impedance scaling

It is generally possible to adapt the noise performance of a given circuit topology with little development effort. Every impedance and transconductance needs to be scaled by the same factor. This scales power consumption (9) and signal-to-noise ratio (12) by that factor. Noise variance is scaled by that same factor while noise magnitude (3) is scaled by the square root of the factor. The mechanism is called impedance scaling.

3.3 Digital signal processing

Digital signals suffer from the same noise and technology limitations as analog and amplitude-continuous time-discrete signals. However, in current processes their integrity is generally not affected by them. There are two reasons for this.

First, there are minimum feature sizes that result in relatively large parasitic capacitance at all digital signal nodes. The error voltage (9) will be orders of magnitude smaller than the signal range, resulting in a negligible chance of misinterpretation. Second, in typical digital circuits the signals are regenerated at every node.

3.4 Information and signal processing

The purpose of signal processing is handling the corresponding information. Amounts of information and their relation with energy is discussed. This is done in order to be able to consider the efficiency of an ADC related to energy and amount of information.

3.4.1 Fixed amount of information and information rate

Signals can consist of discrete symbols or some continuous quantity. A set of discrete symbols can represent a fixed amount of information $N[bits]$. When there is not such a set it can be more practical to define an information rate. An information rate R_H can be defined as the product of the amount of information and the cycle rate (14).

$$R_H = N \cdot f[bits/s] \tag{14}$$

3.4.2 Maximum amount of information

Hartley described the maximum amount of information that can be represented by *l* symbols that all have *s* discrete possibilities by formula (15). The amount is reached when for every symbol all *s* possibilities have the same chance of occurring. The unit in this formula is bit, because 2 is used as the base number of the logarithm.

$$N_{max} = \log_2(s^l) = l \cdot \log_2(s)[bits] \tag{15}$$

In theory an amplitude continuous quantity has an infinite number of possible values. That would make the amount of information that could be represented infinite as well. In nature there is always a mechanism limiting the number of distinguishable values. An electrical quantity is accompanied by a Gaussian noise component. As a result the amount of information that can be represented by an instantaneous electrical quantity depends on the desired certainty.

Shannon defined the channel capacity C. If the information rate R_H is lower than the channel capacity a theoretical coding exists such that any desired certainty can be achieved (16). Shannon derived (17) for a communication channel with additive white Gaussian noise.

$$R_H < C[bits/s] \tag{16}$$

$$C = B \cdot \log_2(1 + SNR)[bits/s] \tag{17}$$

3.4.3 Energy and amount of information - Shannon

For a large SNR Shannon's formula for channel capacity can be approximated by (18). Using formula (13) gives (19). It is now stated that R_H is proportional to C (20), which is approximately true for a constant modulation. Formula (21) results by inserting formulas (11), (14) and (20) into (19). It is the energy of a symbol with information N. The energy per bit is proportional to (22).

$$C \overset{SNR \gg 1}{\approx} B \cdot \log_2(SNR)[bits/s] \tag{18}$$

$$P \propto B \cdot 2^{C/B}[W] \tag{19}$$

$$R_H \propto C[bits/s] \tag{20}$$

$$E \propto \frac{B}{f} \cdot 2^{N \cdot f/B}[J] \tag{21}$$

$$E \propto \frac{B}{N \cdot f} \cdot 2^{N \cdot f/B} = \frac{B}{R_H} \cdot 2^{R_H/B}[J] \tag{22}$$

Shannon also derived from formula (17) that the highest ratio between channel capacity and power is obtained for a very low SNR. Formula (23) is a first order Taylor approximation valid for a small SNR. Combining (23) and (13) yields (24). Formula (25) results by inserting formulas (11), (14) and (20) into (24). The energy per bit does not depend on the number of bits.

$$C \overset{SNR \ll 1}{\approx} \frac{B \cdot SNR}{\ln(2)}[bits/s] \tag{23}$$

$$C \approx \frac{P}{N_0 \cdot \ln(2)}[bits/s] \tag{24}$$

$$E \propto N[J] \tag{25}$$

3.4.4 Energy and amount of information - time-discrete

Formula (21) is not valid for a DC signal because a DC signal does not have a bandwidth. The number of voltage levels that can accurately be distinguished can be doubled by decreasing σ_V by a

factor of two. It yields one extra bit of information (15). Impedance scaling tells that the energy is quadrupled. This reasoning results in (26). The actual proportionality constant depends on the desired certainty.

$$E \propto 4^N [J] \tag{26}$$

3.4.5 Energy and amount of information - digital

For simple digital signal processing the amount of energy required is a linear function of the amount of information. This is because both energy and information processed scale linearly with both operating frequency and number of parallel processing units.

3.4.6 Energy and amount of information - comparison

Formulas (21) and (26) are for amplitude-continuous processing with a high SNR. Energy is an exponential function of the amount of information. For analog signal processing with a low SNR the relation is more favorable and linear (25). For digital signal processing the relation is linear as well. As a result high precision signal processing generally requires less energy in the digital domain.

3.5 Analog-to-digital conversion

First the relation between the number of bits and signal-to-noise ratio is discussed. It is generalized to the relation between effective number of bits and signal-to-noise-and-distortion. A widely accepted benchmark is introduced and subsequently compared to fundamental limitations.

3.5.1 SNR and number of bits

As discussed in paragraph 3.4.4 energy is an exponential function of the number of bits. It is equivalent to state that energy expressed in decibels is proportional to the number of bits. For a converter processing a full swing sine wave formula (27) is often used. This formula is linear instead of truly proportional.

$$SNR \approx 1.76 + 10 \cdot \log_{10}(4^N) \approx 1.76 + 6.02 \cdot N [dB] \tag{27}$$

3.5.2 Effective number of bits and figure of merit

Formula (27) can be inverted to calculate the effective number of bits (ENOB) of a converter. The signal-to-noise-and-distortion (SINAD) is used to take both noise and other factors reducing signal integrity into account (28). In this formula the SINAD is expressed in decibels. Offset and gain error are not taken into account. For some applications these are of minor importance, for example audio or video processing.

$$ENOB = \frac{SINAD - 1.76}{6.02} [bits] \tag{28}$$

A figure of merit (FOM) has been defined for analog-to-digital converters. Its general form is (29), which can be replaced by (30) if an ADC achieves its ENOB at its full sample rate.

$$FOM = \frac{P}{2^{ENOB} \cdot 2 \cdot B} [J / conversion - step] \tag{29}$$

$$FOM = \frac{E}{2^{ENOB}} [J / conversion - step] \tag{30}$$

3.5.3 Comparison of FOM with limitations

An ADC is a bridge between analog and digital signal processing and as such contains both analog and digital circuitry. It handles one symbol with N bit information at a time. Consequently, a part of its energy consumption is proportional to 4^N, paragraph 3.4.4, and a part is proportional to N, paragraph 3.4.5. Formula (31) contains these limitations. A more accurate model would also include other factors and minimum feature sizes. Formula (32) gives the FOM according to (30) under the assumption that the ADC can be scaled like (31).

$$E_{total} = E_{analog} + E_{digital} = E_{analog,0} \cdot 4^N + E_{digital,0} \cdot N [J] \tag{31}$$

$$FOM_{assumpt} = E_{analog,0} \cdot 2^N + E_{digital,0} \cdot N \cdot 2^{-N} [J / conversion - step] \tag{32}$$

If formula (30) would correspond to the fundamental limitations formula (32) would not be a function of N. The FOM suggests a proportionality of 2^N instead of 4^N and N. It can be concluded that the FOM does not correspond to analog or digital fundamental limitations. It does not correspond to the Shannon limit (21) either.

Still the FOM can result in a good fit. A first mechanism that can lead to a fit is that 2^N is somewhat in between N and 4^N. A second mechanism is that ADC developers can work towards a FOM that fits in the FOM trend. An attractive property of the FOM is its simplicity.

4 Scope of an ADC

In this project design specifications may be picked to facilitate low-power design. There is an obvious case for removing circuitry that needlessly dissipates energy. This makes it relevant to consider when an integrated circuit can reasonably be called an ADC.

In this chapter there will be decided upon conditions that can be argued to be reasonable. This includes a set of essential functions, paragraph 4.1, minimum specifications, paragraph 4.2 and reference requirements, paragraph 4.3. Of course reasonability is very subjective.

4.1 Essential functions

One possible definition of an ADC is a circuit that performs both amplitude and time discretization. The following paragraphs will go further into detail.

4.1.1 Amplitude discretization and digital output

As discussed in paragraph 3.1, a digital signal is a discrete signal. It could be argued that a circuit that merely performs discretization is an analog-to-digital converter. A more common conception of an ADC is that of a circuit that codes its output using a different set symbols. Binary signals are commonly used for the digital output.

It is decided that it is reasonable to conform to the common conception and use a common binary coded output. This allows convenient interfacing and a fair comparison between various converters.

4.1.2 Time discretization

In general an ADC performs both amplitude and time discretization. Time discretization is usually performed by a sample-and-hold circuit. Not every published ADC performs time discretization [1]. For this project it is decided that time discretization is an essential function of an ADC.

A result of time discretization is aliasing. Signal components are indistinguishable from signal components at certain different frequencies. Some components present in the input signal can be unwanted in the output signal. An analog filter can be used to remove these from the input signal. Such an anti-aliasing filter can be integrated into an ADC circuit. For this project it is decided that this is not an essential function of an ADC.

4.2 Minimum specifications

Without a minimum set of specifications circuits that can not reasonably be called an ADC could be qualified as one. There is decided upon a set of minimum specifications to prevent this.

4.2.1 Accuracy

Within a certain band an accuracy of more than one bit should be realized. This specification disqualifies a wire, an inverter, a latch and a flip flop as an ADC. A wire and an inverter have also been disqualified by the requirement of time discretization, paragraph 4.1.2.

4.2.2 Input

Just like for most analog circuits, input impedance can be an important specification of an ADC. If the input impedance is low ohmic and resistive, significant power can be delivered by the input to

the ADC. If the input impedance is dominantly capacitive, very little power is delivered by the input. For this project it is decided that it is undesirable to drain power from the input and that this power should at least be included in the consideration of the ADC power consumption.

4.2.3 Output

In a typical ADC application subsequent signal processing is performed on the same chip. In some applications a chip consists of an ADC only. Driving an external output requires substantially more power than driving an internal output. For this project it is decided that it is reasonable that the ADC should be able to drive an on chip minimum size digital input.

4.2.4 Conversion speed

Any slow ADC can be used as a building block for a fast one. This can be done with distributed sample-and-hold circuitry. It is assumed this is feasible for quite a wide range of applications and that it is therefore not necessary to define a limitation on conversion speed. Note that the figure of merit (30) does not depend on conversion speed.

4.3 References requirements

A large scale integrated circuit often contains reference circuitry. The generated references are shared between many converters and other analog circuits. As such it can be argued that generation of stable references does not need to be included in the ADC energy consumption.

4.3.1 Voltage and current references

As decided in paragraph 4.1.1, amplitude discretization needs to be performed. This discretization requires the input signal to be related to a reference. A simple and low-power ADC implementation could contain 2^N switches and require 2^N accurate and low ohmic voltage references.

For this project it is decided that it is reasonable to require one or a small number of accurate low ohmic voltage references. It is also decided to be reasonable to require a current reference. Of course power delivered by these references needs to be included in the ADC power consumption.

A justification for the reasonability of the voltage references is that for large powers both AC/DC and DC/DC converters can be implemented with a near 100% efficiency. A justification for the current reference is that reasonably well defined resistors are available for VI conversion.

4.3.2 Time or frequency references

As decided in paragraph 4.1.2, time discretization needs to be performed as part of the analog-to-digital conversion. This discretization requires a time reference. In addition, some ADC architectures require a clock signal for their internal operation. An example is a counting ADC.

For several ADC applications the ADC needs to operate coherently to other processing blocks. A typical measurement to determine the SINAD to determine the FOM, paragraph 3.5.2, also uses coherent sampling. An external time reference is required. The relevant specification for coherent operation is on tracking jitter. If the ADC does not need to operate coherently the relevant specification is on period jitter instead.

Similarly to what was decided in 4.3.1, it is decided that it is reasonable to require an external clock signal with a frequency that is equal or similar to the conversion frequency.

5 Low-power ADC implementation

As discussed in chapter 4 every ADC needs to perform time and amplitude discretization and provide a binary coded output. The same functional behavior can be implemented using a variety of architectures. A short overview will be given in paragraph 5.1. Familiarity with analog-to-digital conversion is assumed.

The circuitry performing time discretization is often called a sample-and-hold circuit. Amplitude discretization and binary coding is performed by a combination of level creation, comparison and some digital circuitry. These building blocks are usually not readily distinguishable as such. They are combined and split up aiming at various advantages. The distinguished functions are discussed. The demands of several ADC architectures on the functions will be qualitatively compared.

In general low-power conversion requires all of the functions to be low-power. Trade-offs exist. In paragraph 5.6 trade-offs are indicated and one architecture is selected for further work.

5.1 Overview of ADC architectures

Various ADC architectures exist. Categories can be defined to create an overview. In this work the categories are direct conversion, linear approximation and logarithmic approximation. It is just one possible set of categories.

5.1.1 Direct conversion

A direct conversion ADC performs an N bit conversion in one cycle. A flash ADC belongs to this category. A folding ADC can also be regarded as a direct conversion ADC. It has properties of a subrange ADC as well.

5.1.2 Linear approximation

A linear approximation ADC performs an N bit conversion in 2^N cycles. During every cycle one of the 2^N possible binary codes is examined as the most accurate one. Examples of this architecture are dual slope and counting ADCs.

5.1.3 Logarithmic approximation

A traditional logarithmic approximation ADC performs an N bit conversion in N cycles. A generalization is that the amount of output information is proportional to the amount of cycles. The traditional definition covers subrange ADCs. The generalization also covers sigma delta ADCs.

A pipelined ADC is a subrange ADC. N stages are used for N output bits. A successive approximation register ADC (SAR) is a subrange ADC that uses one stage for all output bits. A subrange ADC can always be extended with an over-range mechanism. A 1.5 bit ADC is a pipelined ADC with over-range.

A folding ADC is in fact a subrange ADC that does not use an extra cycle to create subranges. It can be faster at the cost of increased complexity.

5.1.4 Selection of architectures

In this chapter a qualitative comparison will be made of suitability of ADC architectures for low-power conversion. Instead of comparing all architectures a representative selection will be made

first. Direct conversion architectures will be represented by the flash architecture. Linear approximation architectures will be included as one category. Logarithmic approximation architectures will be represented by sigma delta, 1.5 bit and SAR.

5.2 Sample-and-hold circuitry

The minimum functionality of sample-and-hold (SH) circuitry is time discretization. Additional functionality can be buffering, filtering or amplification, as required by some applications or architectures. A minimum functionality circuit diagram of a SH for an ADC with an analog voltage input is shown in figure 1. As a side note, a more correct classification of this circuit is track-and-hold circuit.

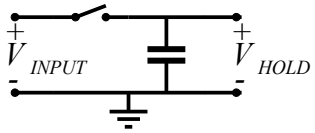

Figure 1: minimum functionality SH

In ideal switches and capacitors no power is dissipated. In an actual CMOS implementation the switch can be a transistor in deep triode. Its minimum power dissipation heavily depends on technology limitations.

No architecture has a significant advantage in its sample-and-hold circuitry. That is why no architecture comparison is included here.

5.3 Level creation

As mentioned in paragraph 4.3.1, the input signal needs to be related to a reference. Signal processing needs to be performed on input, reference or both. In this work, the processing is called level creation. Often it is voltage level creation. Because of the level creation, it can be argued that an ADC always contains some form of digital-to-analog conversion.

For a flash ADC all 2^N voltage levels need to be available at the same time. Usually a voltage division mechanism consisting of resistors is used. For a linear approximation ADC all 2^N voltage levels need to be available subsequently. A counter can be used in combination with a current source and a capacitor. A 1.5 bit ADC requires both accurate addition and amplification. It is commonly implemented using switched capacitor circuitry. A simple SAR needs N levels to be available subsequently and can use a general digital-to-analog converter (DAC) in its feedback loop.

A simple sigma delta ADC uses two accurate external reference voltages and an analog feedback loop. Through a subtraction point the reference voltages are loaded with the feedback loop. The feedback loop itself contains most of the level creation complexity.

The amount of energy required for level creation depends on the amount of levels that need to be created and on the creation mechanism. Table 1 contains a qualitative comparison of energy requirements between several architectures.

Function	Architecture				
	Flash	Linear approximation	Sigma delta	1.5 bit	SAR
Level creation	High	Moderate	Moderate	Moderate	Low

Table 1: Qualitative comparison of level creation energy requirements

5.4 Comparison

Levels created by level creation circuitry need to be compared. An ADC contains one or more comparators. The output of an ideal comparator is amplitude discrete and uniquely determined by its inputs. Imperfections, their effects and the subsequent power dissipation are discussed in the following paragraphs.

5.4.1 Comparator imperfections

The main imperfections of a comparator are its limited speed and its inaccuracy. The magnitude depends on comparator architecture, technology limitations and fundamental limitations. Inaccuracy can be divided into offset and noise. On a system level these can best be described as input-referred quantities.

Offset and a limited speed are a direct result from technology limitations. Maximum speed depends mostly on the presence of parasitic capacitances. Noise is a fundamental limitation. In addition to fundamental noise a comparator can both generate and be sensitive to supply noise. Supply noise is an engineering issue.

5.4.2 Effects of comparison imperfections

The system level effects of comparator inaccuracies depend heavily on the ADC architecture. The speed of a comparator can limit the conversion speed of an ADC. This imperfection is mostly ignored for this project as discussed in paragraph 4.2.4.

For a SAR ADC the comparator offset is the ADC offset. This offset is acceptable for some applications as discussed in paragraph 3.5.2. Noise can be the limiting factor on the SINAD. In a sigma delta converter offset has very little effect on converter accuracy. Noise is shaped by a loop filter. A 1.5 bit converter uses an over-range mechanism such that offset and noise of the comparators in the first stages do not affect the output. Comparator offset and noise in the last stage have little effect on the output due to the amplification in the previous stages.

A flash ADC requires 2^N comparators for 2^N comparisons. Both offset and noise of all comparators need to correspond to the full accuracy of the ADC. A linear approximation ADC also requires 2^N comparisons but needs only one comparator.

5.4.3 Comparison power dissipation

It is convenient to judge a comparator on its energy consumption per comparison instead of on its continuous power consumption. Formula (11) can be used. Comparator energy dissipation depends on a combination of comparator architecture, required specifications and technology. Comparison energy dissipation depends on comparator energy and on the number of required comparisons. Table 2 contains a qualitative comparison of energy requirements between several architectures.

	Architecture				
	Flash	Linear approximation	Sigma delta	1.5 bit	SAR
Comparisons per conversion	High	High	Low	Low	Low
Energy per comparison	High	High	Low	Low	High
Energy per conversion	High	High	Low	Low	Moderate

Table 2: Qualitative comparison of comparison energy requirements

5.5 Digital circuitry

Digital circuitry can be required in an ADC control path. Additional digital circuitry can be required for the digital output. The first digital signals in an ADC are the comparison output signals. In paragraph 4.1.1 it has been decided that the output should use a common binary coding. Digital circuitry generates the common binary coding based on the comparison output. The complexity strongly depends on the ADC architecture.

The digital circuitry for a linear approximation ADC commonly contains a simple binary counter. This counter also provides a common binary coding. Therefore these three architectures can directly provide the desired ADC output.

The comparison output in a flash ADC is a thermometer coded value. Due to comparison errors there can be a bubble, an inconsistency in the code. As a result multiple comparison outputs map onto the same ADC output. The same is the case in an ADC with over-range, like a 1.5 bit converter. For flash and over-range converters simple combinational logic is required to recode the comparison output.

The serial comparator output of SAR ADC is a common binary coding. The serial comparator output of a sigma delta ADC could also be argued to be a common binary coding. A decimation filter is required if it is desired to convert the sigma delta output to the same common binary coding as other converters.

Energy dissipated in the digital circuitry depends both on the complexity and the amount of required digital processing. Table 3 contains a qualitative comparison of energy requirements between several architectures. For the sigma delta converter it is assumed that a decimation filter is not required. If it is, the energy requirements would be high.

Function	Architecture				
	Flash	Linear approximation	Sigma delta	1.5 bit	SAR
Digital circuitry	Moderate	Moderate	Low	Moderate	Low

Table 3: Qualitative comparison of digital circuitry energy requirements

More advanced schemes for digital error correction can be implemented, including digital data analysis. Such schemes are basically implemented on top of a basic architecture and are therefore not taken into account in this architecture comparison.

There are some general methods to decrease power consumption of digital circuitry at the cost of speed. The dominant power consumption usually results from charging and discharging all parasitic capacitances. The parasitic capacitances can be minimized by using the smallest allowed feature sizes for all transistors. In formula (10) it can be seen that the energy is proportional to V^2. Consequently a reduction of the supply voltage can reduce the energy consumption.

Energy is also dissipated during the time that the digital input of a digital cell is in between the supply voltages. This dissipation can be reduced by reduction of the supply voltage too. If further reduction of the supply voltage is undesirable transistors with a high threshold voltage can be used.

5.6 Comparison of architectures

Function	Architecture				
	Flash	Linear approximation	Sigma delta	1.5 bit	SAR
Level creation	High	Moderate	Moderate	Moderate	Low
Comparison	High	High	Low	Low	Moderate
Digital circuitry	Moderate	Moderate	Low	Moderate	Low

Table 4: Qualitative comparison of energy requirements

The architectures from paragraph 5.1.4 have been compared in table 4. The three most promising ones for low-power analog-to-digital conversion are logarithmic approximation architectures. This project focuses on SAR converters. It is a promising architecture and there has been an innovation in the area of comparators shortly before the start of this project [2].

6 Low-power successive approximation ADC

First the basic principle of a successive approximation ADC is discussed in paragraph 6.1. Next techniques on the converter architecture level are discussed for potential comparison energy reduction in paragraph 6.2. Paragraph 6.3 discusses charge redistribution level creation and techniques to potentially reduce energy dissipation for it. A new energy-efficient comparator is introduced in paragraph 6.4.

6.1 Basic principle

Figure 2 contains a diagram of a basic SAR ADC. Prior to an actual conversion there is a sample-and-hold operation and the register is reset to contain only zeros. First the most significant bit (MSB) is tested. This is done by initially setting the MSB of the DAC to one and then comparing if this is either an over-estimation or an under-estimation. The result is stored in the MSB position of the register and consequently the MSB of the DAC is set for the rest of the conversion. The same procedure is followed for all other bits, from most significant to least significant. After N comparisons the register contains the output of an N bit conversion.

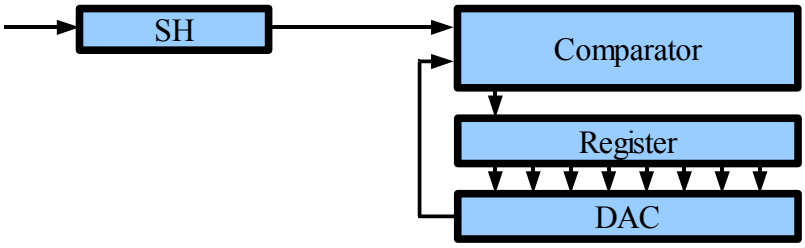

Figure 2: Diagram of a basic SAR ADC

The name of the register, successive approximation register, is commonly used to identify the whole converter. Note that the DAC in the converter requires one less bit than the full ADC.

6.2 Comparison energy reduction

The main weak point of the SAR architecture compared to the sigma delta and 1.5 bit architectures is that every comparison needs to be done at the full ADC accuracy. Architecture level techniques that can possibly reduce the comparison energy will be discussed.

6.2.1 Over-range

A 1.5 bit ADC requires less accurate comparisons than a basic SAR ADC because it uses an over-range mechanism. It is possible to extend a SAR ADC with an over-range mechanism without requiring the same analog addition and multiplication as a 1.5 bit converter. This can be done by connecting several different SAR converters in parallel.

First all converters need to sample the same analog input value. They can all sample independently or use one combined master SH circuit. Next the least accurate SAR ADC performs a conversion. A sub-range of the full ADC input range is determined which includes the input value. From the point of view of the first SAR ADC this sub-range is an over-range, because is larger than its least-significant-bit (LSB).

The next SAR ADC is more accurate than the first one. The range of this converter is the determined sub-range. An arbitrary number of converters can be used subsequently. Only the last converter needs to operate at full accuracy. Because of the over-range mechanism multiple outputs map on the same digital output value. Some combinational logic is required to construct the desired

digital output.

A less accurate ADC can use a less accurate comparator, using less energy per conversion. In addition the level creation circuitry can also be less accurate.

As discussed in chapter 3 processing energy is an exponential function of the accuracy. As a result the energy consumption of the last SAR ADC is dominant. A theoretical energy reduction by a factor of almost N is possible.

Because the consumption in the last ADC is dominant it can be expected that additional energy savings are insignificant if more than two or three parallel converters are used. By further increasing the number of converters the change in energy consumption will depend on the resulting digital complexity.

6.2.2 Smaller average number of comparisons

The Hartley formula (15) gives the maximum amount of information that can be represented by a symbol that has *s* discrete possibilities. In an ADC a symbol is a sample and the *s* discrete possibilities are the 2^N possible input level ranges. The condition that for every symbol all *s* possibilities have the same chance of occurring corresponds to a uniform amplitude distribution and no time correlation. The standard SAR algorithm corresponds to a block encoding which is optimal if this condition is met.

For a practical input signal the condition is often not met and the SAR algorithm is not necessarily optimal. Before and during a conversion the sample can usually be predicted with some accuracy. A simple prediction can merely be based on a known amplitude distribution. For a more advanced prediction the previous samples and autocorrelation function can also be taken into account.

In the standard SAR algorithm every comparison reduces the sample range by 50%. The algorithm would add the maximum amount of information per comparison if a one and a zero would have the same chance of occurring. For a practical input signal this is often not the case. The algorithm can be adapted to add more information per comparison.

In such an adapted SAR algorithm the sample range is not necessarily reduced by 50%. For example it can be reduced by either 10% or 90% based on the comparison. Either way a larger amount of information is added than the expected amount of added information of the standard algorithm.

In 1951 Huffman developed an algorithm to group together the *s* discrete possibilities based on their chance of occurring. He proved this algorithm to be optimal. For an ADC his optimality corresponds to the smallest number of average comparisons required. Huffman coding can combine any possibilities based on their chance of occurring. In an ADC there is the added restriction that the range can only be divided in two ranges smaller and larger than a certain value. As a result the adapted SAR algorithm is not necessarily as efficient as Huffman coding.

A practical implementation can have some similarities with the over-range implementation as described in paragraph 6.2.1. In the over-range case an accurate converter only examines a sub-range. In the adapted SAR algorithm a sub-range is examined first and only if the sample turns out not to be within this sub-range a larger range is examined. It is like a bottom-up approach instead of the top-down-like approach of the standard SAR algorithm.

A side-effect of a smaller average number of comparisons is a smaller average conversion time. However, the maximum conversion time increases. Most practical ADC applications use a fixed sample rate. For a single converter based on this principle the maximum conversion time should be regarded. For an interleaved ADC using several of these converters it is possible to use the average

time plus some margin instead. This can actually result in a faster ADC for the same number of building blocks.

Just like an over-range converter a converter based on a smaller average number of comparisons requires more complex digital circuitry. Its energy consumption is likely higher than in a standard SAR ADC. However if the circuitry is designed event-driven most of the logic gates will not contribute to the energy consumption and the average energy consumption can still be low. Furthermore it can be expected that implementation becomes more favorable as processes scale.

6.2.3 Over-sampling

Both comparator noise and quantization noise are white. Sampling causes all noise to fold to half the sampling bandwidth. Consequently a result of over-sampling is that less noise folds to the original bandwidth. Over-sampling with a factor of n reduces noise power in the band of interest by a factor of n. For example four times oversampling yields one extra bit at the cost of four times more power. This is practically the same increase in power as would be required to get one extra bit of accuracy without over-sampling. Therefore over-sampling by itself does not reduce comparator energy.

When coherent ADC applications is not required the relevant clock generation specification is on period jitter, as discussed in paragraph 4.3.2. For a constant oscillator power and efficiency the absolute period jitter is lower when the output frequency is increased. As a result over-sampling can reduce the effect of clock noise on ADC accuracy.

Other effects of over-sampling have not been taken into account in this consideration. These include linearity, overhead and flicker noise.

6.2.4 Over-sampling with feedback

A sigma delta ADC is an example of an ADC that uses over-sampling in combination with feedback. Every comparison output enters a feedback loop. Normal over-sampling with a factor of n reduces noise power in the band of interest by a factor of n. The loop filter of a sigma delta ADC shapes more of the noise to outside the band of interest. It is called noise shaping and allows a sigma delta ADC to use less accurate comparisons than a SAR ADC.

As discussed in chapter 5 there is a disadvantage of a sigma delta ADC compared to a SAR ADC in its level creation energy. This is because of its analog feedback loop. The loop can be a higher load for a DAC than a comparator and the loop itself dissipates energy.

It is theoretically possible to move the feedback loop to the digital domain. The resulting ADC would be a hybrid of a sigma delta ADC and a SAR ADC. Its basic diagram would be like figure 2 where the register is replaced by a more complex digital block.

The feedback loop is more or less approximating the current sample. In that regard it is similar to reducing the average number of comparisons as described in paragraph 6.2.2. Depending on the input signal the optimal feedback filter is most likely not linear.

The main disadvantage of this hybrid is that the inherent linearity of a one bit DAC is more difficult to achieve for a high resolution DAC as required in this hybrid. A solution could be sought in the directions of calibration or digital data analysis. This is a recommendation for future work.

6.3 Charge redistribution level creation for SAR

Various level creation architectures based on charge redistribution are discussed in this section. The common factors are voltage division with capacitors and the resulting capacitive output. Such an

output is suitable for a capacitive input, like the gate of a MOST. Various comparator architectures exist with such an input.

6.3.1 Two-capacitor architecture

A charge redistribution architecture based on two equally sized grounded capacitors has been described in literature in 1974 [3]. The same authors wrote an improved paper in 1975 [4]. One of the capacitors is alternating switched to one of two references and to the other capacitor.

A digital-to-analog conversion always starts with the least significant bit and finishes with the most significant one. This order is reversed compared to the SAR algorithm.

6.3.2 Traditional weighted-capacitor architecture

A charge redistribution architecture based on binary weighted capacitors has been described in literature in 1975, partially by the same authors who described the two-capacitor architecture [5]. The top terminals of all capacitors are connected together. A diagram of the traditional weighted-capacitor architecture is shown in figure 3.

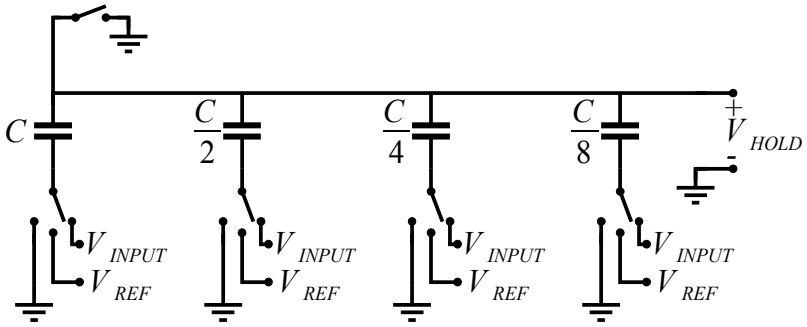

Figure 3: Traditional weighted-capacitor architecture

During hold mode all bottom terminals are connected to one out of two reference voltages. In figure 3 the ground terminal is one of the two references. During redistribution mode the bottom terminal of one of the capacitors will be switched from one reference to the other. This capacitor is called the control capacitor $C_{control}$. There can be a parasitic capacitance between the combined top terminal and other nodes. In equation (33) the total capacitance is subdivided into four corresponding categories.

$$C_{total}=C_{ref1}+C_{ref2}+C_{control}+C_{parasitic}[F] \tag{33}$$

The voltage at the combined top terminal will now deterministically be modified by switching from one reference to the other. The change is a linear function of the difference between both reference voltages, formula (34). Note that not the shape of its path but the magnitude of the voltage influences the change in output voltage.

$$\Delta V_{HOLD}=\pm V_{REF}\cdot\frac{C_{control}}{C_{total}}[V] \tag{34}$$

An implicit control voltage can be defined. It is the voltage at the bottom terminal of the control capacitor. The voltage drop over parasitic switching resistances is the difference between the reference voltages and the implicit control voltage.

During the sample mode of a SAR based on this architecture all bottom terminals are connected to the input voltage V_{INPUT} and the top terminal is connected to a reference voltage. To go from sample mode to hold mode first the top terminal is disconnected. Next the MSB capacitor is connected to

the positive reference while all other capacitors are connected to the negative reference. Energy is dissipated in the level creation even before the first comparison.

The top terminal is both during sample mode and at the end of the conversion at a voltage close to the reference voltage. A resulting advantage is that there is hardly a gain error introduced by parasitic capacitances.

A disadvantage is the complex switching for the sample-and-hold operation. It needs to be possible to connect every bottom capacitor terminal to both reference voltages and the input voltage. For low distortion it is important that input resistance and switch-timing are sufficiently level-independent.

6.3.3 Alternative weighted-capacitor architecture

The complexity of the sample-and-hold operation can be reduced by directly sampling the input voltage on the top terminal. The switching complexity for a bottom terminal can be as low as an inverter.

A disadvantage of the traditional weighted-capacitor architecture is that energy is dissipated in the level creation even before the first comparison.

This first step can be avoided by a level shift of the reference. It is now possible to replace the MSB capacitor by a second set of binary weighted capacitors. Initially all capacitors within a set are connected to the same reference. The two sets start at opposite references. Now any next step in the SAR algorithm requires exactly one bottom terminal to change its reference. Figure 4 shows the alternative architecture.

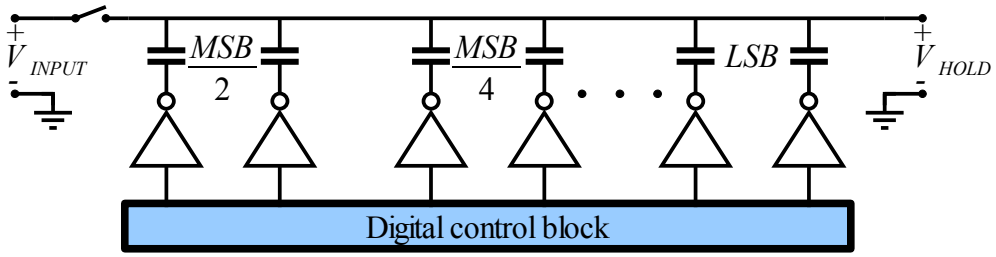

Figure 4: Alternative weighted-capacitor architecture

The figure contains a diagram of the alternative weighted capacitor level creation architecture, including the location of the sample-and-hold switch and a digital control block. The digital control logic is slightly less complex than that in a traditional weighted-capacitor architecture. A first reason is the reduced complexity of the sample-and-hold operation. A second reason is that it is never necessary to switch back a bit that has been switched on for testing as part of the basic algorithm.

6.3.4 Accuracy through settling

Formula (34) assumes that the reference voltages are constant and do therefore not act like additional control voltages. In reality fluctuations in reference voltages influence the hold voltage the same way the control voltage does. Instantaneous hold voltage accuracy depends on instantaneous accuracies of the reference voltages. One of the factors influencing the accuracy of a reference is its output current. This current depends on the load.

During redistribution mode the load is not necessarily well defined. During hold mode it is dominantly capacitive. This is true for all charge redistribution architectures. Redistribution can temporarily disturb the accuracy of a reference. In fully settled hold mode there is no current. By allowing some time for settling the accuracies of the references and consequently the hold voltage can be improved.

Because of the lack of current the references do not deliver any power during hold mode. This property makes charge redistribution architectures attractive for low-power analog-to-digital conversion.

6.3.5 Dissipation during charging and discharging of capacitors

During the redistribution mode of a two-capacitor circuit the load on the control voltage is one of the capacitors. For a weighted-capacitor circuit all capacitors except for the control capacitor are switched in parallel with each other. The control capacitor is switched in series with all other capacitances. The resulting load on the control voltage behaves like one capacitor.

For all architectures charge needs to be added to or removed from a real or equivalent capacitor. The most simple way to charge or discharge a capacitor is to switch a capacitor terminal from one voltage source to another, as shown in figure 5.

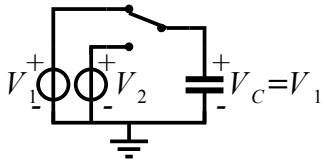

Figure 5: Simple circuit for charging and discharging a capacitor

Energy can only be dissipated in resistances. Most of the dissipation occurs in the parasitic resistances of the switches. The magnitude of the dissipation depends on the capacitance and on the voltage difference. Formula (10) can be used.

A common mode does not influence the amount of dissipation. It does however add some complexity to calculations based on conservation instead of on dissipation. In these calculations voltage sources can deliver energy to each other.

6.3.6 Reduction of dissipation

Energy dissipation happens in resistances and depends quadratically on the voltages across them (9). DC/DC conversion techniques can reduce these voltages. Application can result in considerable less dissipation during charging and discharging of capacitors. One possible technique uses an inductor in series with the switch and the capacitor, as shown in figure 6.

The circuit is shown in a DC steady state, with the top terminal of the capacitor directly connected to one of the voltage sources. A three-phase mechanism is required to charge or discharge the capacitor from V_1 to V_2.

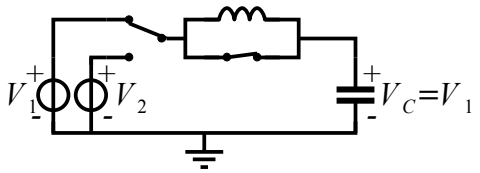

Figure 6: Circuit for charging and discharging a capacitor

The first phase is shown in figure 7. The initial large voltage difference that would otherwise be over a parasitic resistance is now over the inductor. The inductor stores energy. The phase ends when the change in capacitor voltage is halfway in between V_1 and V_2. This moment depends on the values of the inductor and the capacitor. It does not depend on the DC voltage levels. It can be determined by timing.

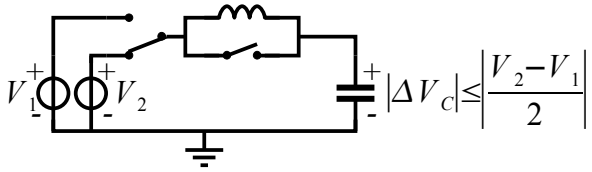

Figure 7: First phase of a charging or discharging operation

The second phase is shown in figure 8. During this phase the energy stored in the inductor is used to further charge or discharge the capacitor. When the capacitor voltage has reached approximately the correct level the second phase ends. This takes the same amount of time as the first phase and can be determined by timing.

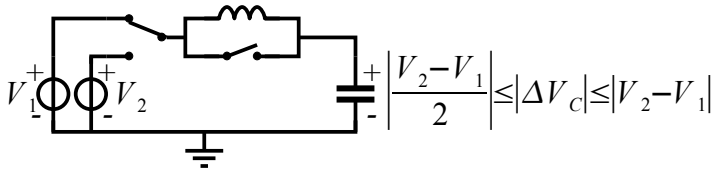

Figure 8: Second phase of a charging or discharging operation

The third phase is shown in figure 9. At the start of this phase there is no more energy stored in the inductor. It can therefore be short circuited without energy loss. The circuit enters another DC steady state. The conversion efficiency depends on the accuracy of the timing. The capacitor voltage accuracy does not depend on the timing. It depends on the accuracy of the references.

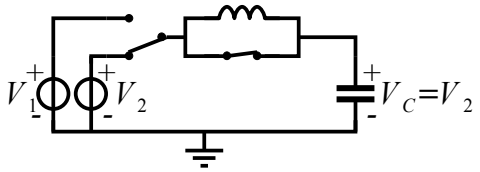

Figure 9: Third phase of a charging or discharging operation

An alternative DC/DC conversion technique is step-wise and uses a number of voltage levels in between both reference voltages. It is shown in figure 10.

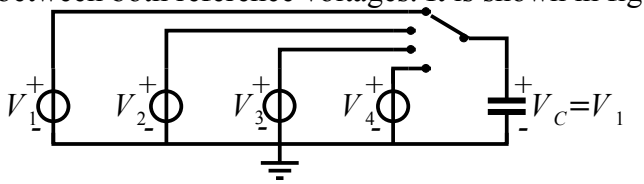

Figure 10: Another circuit for charging and discharging a capacitor

To charge or discharge the capacitor from V_1 to V_4 it is subsequently connected to V_2, V_3 and V_4. When appropriate intermediate levels are used every individual voltage step is small, reducing the voltages across resistances. The energy dissipation in this specific example can be calculated by formula (35). The general case for *n* equidistant steps can be calculated by formula (36).

$$E=\frac{1}{2}\cdot C\cdot\left((V_1-V_2)^2+(V_2-V_3)^2+(V_3-V_4)^2\right)[J] \tag{35}$$

$$E=\frac{1}{2}\cdot C\cdot n\cdot\left(\frac{\Delta V}{n}\right)^2=\frac{1}{2\cdot n}\cdot C\cdot\Delta V^2[J] \tag{36}$$

The conversion efficiency depends on the number and accuracy of the intermediate voltages. The capacitor voltage accuracy does not, it comes directly from the references. If the same intermediate voltage sources are used for both charging and discharging they can be implemented by large capacitors to any supply voltage. During use their charge will automatically converge to appropriate levels.

Both DC/DC conversion techniques are best suited for changing a voltage from one reference to another. Applying them to a weighted-capacitor charge redistribution architecture is straightforward.

The first stage in a two-capacitor architecture charges or discharges from any of many intermediate voltages to a reference voltage. The second stage shorts the two capacitors. As a result it is not so practical to apply either of the DC/DC conversion techniques.

In case of a differential implementation of a weighted-capacitor charge redistribution mechanism two equivalent capacitors need to charge or discharge at the same time. These equivalent capacitors are of equal size and in fact need to swap their charge. A two-phase DC/DC conversion technique similar to the three-phase inductor based single ended technique can be implemented. During the first phase an inductor is temporarily switched in between both equivalent capacitors. During the second phase the equivalent capacitors are switched towards their new references.

6.3.7 Thermal noise lower limit on capacitor value

When a voltage is sampled onto a capacitor thermal noise causes an error voltage (8). For application in an ADC this error voltage needs to be related to the LSB voltage, for example by equation (37). The LSB voltage is related to the total range of the converter (38). Combining these equations gives a minimum value for the hold capacitor (39).

$$\sigma_v \leqslant \frac{V_{LSB}}{2}[V] \tag{37}$$

$$V_{LSB} = V_{RANGE} \cdot 2^{-N}[V] \tag{38}$$

$$C \geqslant \frac{4 \cdot k \cdot T}{V_{RANGE}^2} \cdot 4^N[F] \tag{39}$$

6.3.8 Matching lower limit on capacitor value

Mismatch between capacitors causes non-linear level creation. This is true for both two-capacitor and weighted-capacitor architectures. In this section the non-linear behavior of weighted-capacitor architectures is considered. Similar to what was done in paragraph 6.3.7 the error voltage is related to the LSB voltage and a minimum value for the capacitor is calculated.

Equation (40) is a simplified version of equation (33) and equation (41) is based on (34). The relative output voltage V_{rel} depends on the fraction C_h of C_{total} that is connected to the high reference voltage. Its range is from 0 to 1.

$$C_{total} = C_h + C_l[F] \tag{40}$$

$$V_{rel} = \frac{V_{out}}{V_{RANGE}} = \frac{C_h}{C_h + C_l}[] \tag{41}$$

The capacitor value variances of both capacitors are considered to be independent. This is used to calculate the variance in relative output voltage, formula (42).

$$\sigma_{V_{rel}}^2 = \left(\frac{\partial V}{\partial C_h}\right)^2 \cdot \sigma_{C_h}^2 + \left(\frac{\partial V}{\partial C_l}\right)^2 \cdot \sigma_{C_l}^2[] \tag{42}$$

The partial derivatives are calculated and formula (2) is used for the capacitor value variances. This

directly results in formula (43). More elaboration results in formula (44).

$$\sigma_{V_{rel}}^2 = \left(\frac{(C_h + C_l) - C_h}{(C_h + C_l)^2} \right)^2 \cdot A_C^2 \cdot C_h + \left(\frac{-C_h}{(C_h + C_l)^2} \right)^2 \cdot A_C^2 \cdot C_l [\,] \tag{43}$$

$$\sigma_{V_{rel}}^2 = \frac{C_l^2 \cdot C_h}{(C_h + C_l)^4} \cdot A_C^2 + \frac{C_h^2 \cdot C_l}{(C_h + C_l)^4} \cdot A_C^2 [\,] \tag{44}$$

Formulas (40) and (41) are used to simplify formula (44). This results in formula (45) and with some more elaboration in (46). Note that the variance is zero for a relative voltage of 0 or 1. This corresponds to the strict definition of the INL. Therefore it is an overestimation for the calculation of the FOM as discussed in 3.5.2.

$$\sigma_{V_{rel}}^2 = (1 - V_{rel})^2 \cdot V_{rel} \cdot \frac{A_C^2}{C_{total}} + V_{rel}^2 \cdot (1 - V_{rel}) \cdot \frac{A_C^2}{C_{total}} [\,] \tag{45}$$

$$\sigma_{V_{rel}}^2 = \frac{A_C^2}{C_{total}} \cdot (V_{rel} - V_{rel}^2) [\,] \tag{46}$$

In formula (46) the variance in relative voltage depends on the relative voltage. If the probability density of V_{rel} is known the expected value of $\sigma_{V_{rel}}^2$ can be calculated. Formula (47) is based on a uniform probability density.

$$E(\sigma_{V_{rel}}^2) = \int_{V_{rel}=0}^{V_{rel}=1} \frac{A_C^2}{C_{total}} \cdot (V_{rel} - V_{rel}^2) \, dV_{rel} = \frac{A_C^2}{6 \cdot C_{total}} [\,] \tag{47}$$

The variance in capacitor value is a stochastic process. However it is generally not stochastic in between the creation of various levels. This is because there is only one realization which is determined at the time of manufacturing. As a result the actual variance is smaller in some circuits and larger in others. Several techniques exist to make sure that the variance is smaller than a desired maximum value.

A first technique is arranging the realization to be stochastic in between the creation of levels. This requires all capacitors to interchange roles in a manner unrelated to the signals being processed. A second technique is calibration.

A third technique is static matching. It is assumed that the actual value is a number of times larger than its standard deviation. Parameters are chosen in such a way that the circuit works within specification for the larger value. When the actual value is even larger the circuit has failed proper manufacturing and is scrapped. In equation (48) the parameter is called M.

$$M \cdot \sigma_{V_{rel}} = \frac{M \cdot A_C}{\sqrt{6 \cdot C_{total}}} [\,] \tag{48}$$

Static matching is the easiest technique to implement. It the remainder of this paragraph static matching is assumed. The error voltage needs to be related to the LSB value. Equation (49) is very similar to equation (37). It states that the error voltage should be smaller than half the LSB value. Equation (50) follows from inserting formulas (38) and (48). Equation (51) is an elaborated version of equation (50).

$$M \cdot \sigma_{V_{rel}} \cdot V_{RANGE} \leqslant \frac{V_{LSB}}{2} [V] \tag{49}$$

$$\frac{M \cdot A_C}{\sqrt{6 \cdot C_{total}}} \leqslant 2^{-(N+1)} [\,] \tag{50}$$

$$C_{total} \geqslant \frac{2}{3} \cdot M^2 \cdot A_C^2 \cdot 4^N [F] \tag{51}$$

Calculating an actual minimum value requires numerical values for M, A_C and N. The value in (52) is based on 3σ matching, 1% mismatch for a 1fF capacitor and a 10 bit converter.

$$C_{total} \geqslant \frac{2}{3} \cdot 3^2 \cdot 10^{-19} \cdot 4^{10} \approx 630 [fF] \tag{52}$$

6.3.9 Comparison of lower limits

A lower limit on the capacitor value has been determined for thermal noise and for matching. Which of the effects is dominant depends on the parameters. From (39) and (51) it can be derived that the effects are equal under condition (53). As expected there is no dependence on the number of bits. In (54) the parameters have been replaced by values that can be argued to be realistic for a current project. Mismatch is dominant over thermal noise if the converter range is larger than this value.

$$V_{RANGE} = \frac{\sqrt{6 \cdot k \cdot T}}{M \cdot A_C} [V] \tag{53}$$

$$V_{RANGE} \approx \frac{\sqrt{6 \cdot 1.38 \cdot 10^{-23} \cdot 300}}{3 \cdot 10^{-9.5}} \approx 170 [mV] \tag{54}$$

6.4 Comparator

As discussed in paragraph 5.4.2 the most relevant property of a comparator for a basic SAR ADC is its input-referred noise. Speed and offset are of less importance.

6.4.1 Architectures

Comparator architectures exist with and without a bias current and with and without an externally applied clock signal. An example of a comparator with a bias current and without a clock signal is a high gain differential voltage amplifier. The high gain results in an output that can clip to one of the supply voltages. This traditional approach is still in use [1].

Other comparators use an externally applied clock signal to activate a positive feedback mechanism within an amplification stage. The result is an output that has more reliably assumed a valid digital value. The reliability depends on the gain, the capacitance and the time [6].

A new comparator architecture without a bias current and with an externally applied clock signal has recently been developed as part of the nano-wire project [2]. It has a high speed and a reasonably low input-referred noise for its energy consumption.

6.4.2 New comparator topology

As part of this project yet another new comparator architecture has been developed. It is based on the comparator of the nano-wire project. It is shown in figure 11.

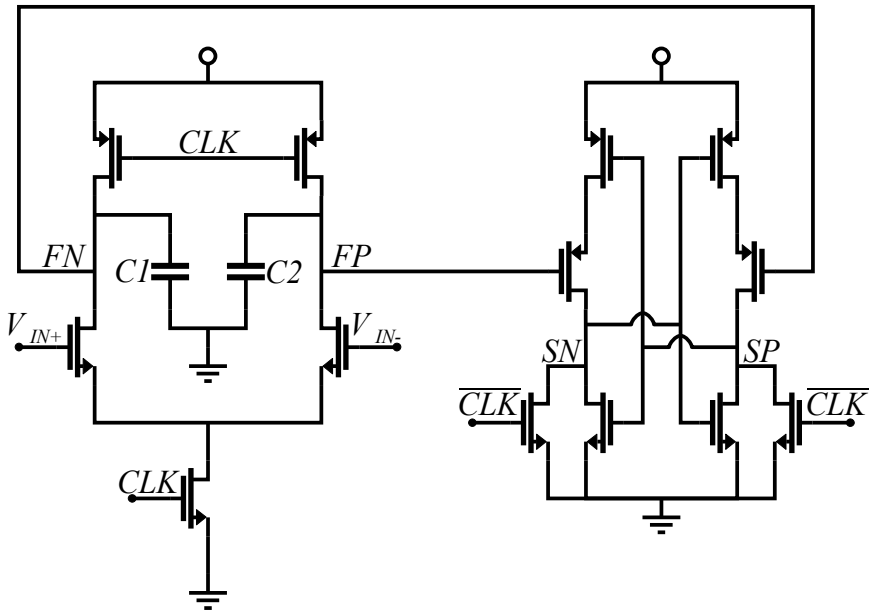

Figure 11: Schematic of new comparator

Like the nano-wire comparator it consists of two stages. Contrary to the first stage of the nano-wire comparator explicit capacitors have been added to nodes *FN* and *FP* . The second stage uses a pair of PMOS transistors within the cross coupled inverters. The nano-wire comparator uses NMOS transistors parallel to the inverters, leading to faster regeneration.

Both comparators can cause some common mode charge injection into the input. This is a result from the tail node that is not precharged. An extra precharge transistor could prevent this at the cost of higher energy consumption.

6.4.3 Operation and gain calculations

While the clock signal is negative nodes *FN* and *FP* are precharged high and nodes *SN* and *SP* are precharged low. On a rising edge of the clock signal the precharging stops and *FN* and *FP* start to discharge to ground. The input transistors and the tail transistor are dimensioned such that the input transistors mostly operate in or close to weak inversion. This gives the highest possible ratio between transconductance and bias current.

Formulas (55) and (56) are valid for a time invariant transconductance *gm* and a time invariant bias current I_{bias} . The bias current I_{bias} is the total tail current and *C* is the total capacitance at nodes *FN* and *FP* combined.

$$v_{out}=v_{FP}-v_{FN}=-1\cdot(v_{IN+}-v_{IN-})\cdot gm\cdot t/(\frac{1}{2}\cdot C)=-1\cdot v_{in}\cdot gm\cdot t/(\frac{1}{2}\cdot C)[V] \tag{55}$$

$$V_{out}=-1\cdot\frac{V_{FP}+V_{FN}}{2}=-I_{bias}\cdot t/C[V] \tag{56}$$

By dividing (55) and (56) on each other a small signal gain depending on output voltage instead of time is derived (57). For (55) and (56) it was initially assumed that the transconductance and bias current are time invariant. This assumption is replaced with the assumption that the pair operates in

weak inversion and that therefore their ratio is constant. Now approximation (58) follows from formula (6) and the fact that I_{bias} is twice the current through one of the input transistors.

$$A=\frac{v_{out}}{v_{in}}=2\cdot\frac{gm}{I_{bias}}\cdot V_{out}[\,] \tag{57}$$

$$A\approx\frac{V_{out}}{m\cdot V_{th}}[\,] \tag{58}$$

A gain from the first stage to the second stage can also be derived. A first convenient approximation is that the input pair of the second stage is off until the input voltage has almost reached the threshold voltage. A second convenient approximation is that subsequently the input voltage drops slow enough for the pair to operate in weak inversion.

Under these approximations the appropriate V_{out} for (58) is the threshold voltage of the second stage. Furthermore expression (58) is also valid for the second stage where V_{out} is the voltage at which the regenerating behavior becomes dominant.

The approximations for this second stage can be made reasonably valid by making the first stage sufficiently slow, but not too slow.

Compared to the nano-wire comparator this comparator can be dimensioned for a considerable higher gain of especially the first stage to the second stage. As a result less regeneration is required. Especially at small input voltages it also has a smaller crowbar current in the second stage. The main disadvantage is that it is slower.

6.4.4 Noise calculations

There are initial noise voltages presents at all precharged nodes. Their input-referred value can be calculated by dividing through the appropriate gain. Equation (59) gives the added noise of the differential nodes FN and FP. The factor of 2 is the combination of two factors of $\sqrt{2}$, one because C is split in two parts and one because the two contributions are added up.

$$\sigma_v\approx 2\cdot\sqrt{\frac{k\cdot T}{C}}\cdot\frac{m\cdot V_{th}}{V_{out}}\approx 4\cdot\sqrt{\frac{k\cdot T}{C}}\cdot\frac{V_{th}}{V_{out}}[V] \tag{59}$$

The noise contribution of the input pair can be calculated with formula (7). The bandwidth needs to be related to a time constant in the system. Formula (60) gives the frequency of the triangle wave that (56) describes the first half of.

$$B\approx\frac{I_{bias}}{2\cdot C\cdot V_{out}}[Hz] \tag{60}$$

Formula (61) enters formula (60) into formula (7). The extra factor of $\sqrt{2}$ is because both input transistors contribute to the noise.

$$\sigma_v\approx\sqrt{2}\cdot\sqrt{\frac{4\cdot k\cdot T}{gm}\cdot B}\approx\sqrt{\frac{8\cdot k\cdot T}{gm}\cdot\frac{I_{bias}}{2\cdot C\cdot V_{out}}}=\sqrt{\frac{k\cdot T}{C}\cdot\frac{I_{bias}/2}{gm}\cdot\frac{8}{V_{out}}}[V] \tag{61}$$

Now approximation (62) follows from formula (61) and (6) and the fact that I_{bias} is twice the current through one of the input transistors.

$$\sigma_v \approx \sqrt{\frac{k \cdot T}{C}} \cdot \sqrt{\frac{8 \cdot m \cdot V_{th}}{V_{out}}} \approx \sqrt{\frac{k \cdot T}{C}} \cdot \sqrt{\frac{16 \cdot V_{th}}{V_{out}}} [V] \tag{62}$$

Comparing formulas (62) and (59) the noise from the input pair is dominant under normal conditions (63).

$$V_{out} \geq V_{th} \approx 26 [mV] \tag{63}$$

Similarly to what was done in paragraph 6.3.7 formulas (37) and (38) are used to give an expression for the minimum capacitor value as a function of the range of the converter.

$$C \geq \frac{4 \cdot k \cdot T}{V_{RANGE}^2} \cdot \frac{16 V_{th}}{V_{out}} \cdot 4^N [F] \tag{64}$$

Calculating an actual minimum value requires numerical values for V_{RANGE}, V_{out} and N. The value in (65) is based on a range of $1\,V$, a threshold voltage of $0.5\,V$ for the input pair of the second stage and a 10 bit converter. The value in (66) is based on a range of $2\,V$ instead.

$$C \geq \frac{4 \cdot 1.38 \cdot 10^{-23} \cdot 300}{1^2} \cdot \frac{16 \cdot 26 \cdot 10^{-3}}{0.5} \cdot 4^N \approx 14 [fF] \tag{65}$$

$$C \geq \frac{4 \cdot 1.38 \cdot 10^{-23} \cdot 300}{2^2} \cdot \frac{16 \cdot 26 \cdot 10^{-3}}{0.5} \cdot 4^N \approx 3.6 [fF] \tag{66}$$

The input-referred noise contributions of the second stage follow the same expressions. The input pair is again dominant over the initial noise voltages at nodes SN and SP. Input-referred the noise of the second stage is divided by the gain of the first stage. As a result the noise of the first stage is dominant if the capacitance at the second stage is less than A^2 times as small.

Energy consumption of the comparator is directly linked to the amount of capacitance that is present. It can be concluded from formula (64) that it is favorable for the comparator energy consumption for the ADC to have a large voltage input range.

Based on these calculations the capacitors C_1 and C_2 have explicitly been added to the architecture. Without them capacitances are implicitly present as part of the various transistors. By placing them explicitly they are present without at the same time introducing an unwanted parasitic. These calculations are based on thermal noise only, during actual dimensioning flicker noise should be taken into account.

6.4.5 Noise simulations

Noise simulations to support or dismiss the noise calculations would be useful. Established noise simulations exist for circuits with a steady state. For the existence of a valid periodic steady state it would be required that the noise is a small signal that does not influence the operating point. Unfortunately when the input signal is small the comparator output is determined by noise rather than by the input signal. Therefore there is no valid periodic steady state in the presence of significant noise.

The alternative is a transient simulation with noise. Both PSTAR and SPECTRE have an option for this. The PSTAR implementation for transient noise is the manual insertion of predefined noise sources at selected nodes. These noise sources can not depend on actual bias conditions of transistors. Because the actual bias conditions of all transistors in the comparator are highly depending on the state of the circuit, this transient noise simulation can not be used.

The transient noise simulation in SPECTRE is designed to automatically take all elements and all time-varying bias conditions into account. Therefore it is a promising candidate for comparator noise simulations. The simulation procedure for comparator noise uses an input signal in the order of the expected input-referred noise. Next the simulation is run a large number of times. From the ratio of correct and incorrect comparator output values the input-referred noise is calculated.

Simulations on MM11 modeled Philips / NXP transistors are at first not functional at all. This problem is fixed in a new version of SPECTRE. Now the simulations run without error but predict a significantly higher noise than the calculations. An incorrect implementation of gate noise error current is identified. This problem is confirmed and further identified at Philips research by people who are very familiar with MM11.

Simulations on a comparator circuit implemented with BSIM4 modeled UMC transistors do initially work. They show a reasonable match with calculations. This is not sufficient information to conclude that either is accurate.

6.4.6 Theoretical further energy reduction

Noise calculations on this comparator give minimum capacitance values. In the current comparator architecture all energy is dissipated. Similarly to what was discussed in paragraph 6.3.6 the amount of dissipation is not fundamentally necessary for correct operation. There should merely be a sufficiently large drain source voltage present for the input pairs to operate in saturation.

The precharge operation on the capacitors in the first stage is an obvious place to apply DC/DC conversion techniques. More reductions are possible. Given the value in formula (65) such measures are probably not worth the added overhead.

This comparator has been developed in CMOS. Some transistors are used in weak inversion to mimic bipolar transistors. Real bipolar transistors could theoretically give better results. If these would be used at the input of the first stage the comparator could only be used once without affecting the hold voltage though. An over-range mechanism as described in 6.2.1 could be applied to overcome this problem.

7 Development of test and demonstration chip

The second project goal is the development of a chip to test and demonstrate some techniques for low-power analog-to-digital conversion. The goals will be further specified in paragraph 7.1. The actual design is discussed in paragraph 7.2. Post layout simulations and results are discussed in paragraph 7.3. Finally future work is discussed in paragraph 7.4.

7.1 Goals

The two goals of the chip are demonstration and test. Both will be discussed in a separate paragraph.

7.1.1 Demonstration

The goal of the demonstration is to demonstrate some of the discussed techniques towards low-power analog-to-digital conversion. Several techniques have been discussed in chapter 6. It is necessary to select a small number of those for actual implementation in an ADC. A first reason for this is that it is desirable that performance can sufficiently easily be attributed to those techniques. For publication it should be possible to describe the ADC and its measurements in a manner that can sufficiently easily be understood in just a few pages.

A second reason is limited development time. It is desirable that the graduation project, including most of the development process, is finished within approximately the nominal time of 25 weeks.

The figure of merit, as described in paragraph 3.5.2, is a widely accepted benchmark for low-power analog-to-digital conversion. For a demonstration with some impact the demonstration ADC should have a significantly lower FOM than currently published converters. It is not a project goal to obtain a FOM that is as low as possible. Presently a state of the art ADC has a FOM in the order of 160 fJ / conversion-step [7].

7.1.2 Test

Actual performance can somewhat be predicted by calculations and simulations. For various reasons the accuracy is limited and it is not possible to calculate and simulate everything. The goal of the test is to find out if and to what extend the ADC and its various building blocks are functional. This goal requires implementation and measurements.

7.2 Design

Major design decisions and boundary conditions specific to this project are discussed here. The boundary conditions discussed in chapter 4 are valid for this project, but not specific to it. Chip layout has been finished. The chip is scheduled to be manufactured on a multi project wafer.

7.2.1 Process

A CMOS 65 nm bulk low-power process is used without additional process options. This process is currently more or less standard for development at NXP. Especially the small feature sizes and the reasonably well controlled high accuracy make this process suitable for the development of a low-power ADC.

7.2.2 Design for testability

In order to be able to test the ADC and its various building blocks it is necessary to implement it completely and put it on a chip. The chip has to be put on a test board. As discussed in chapter 4 the scope of the ADC is smaller than the scope of a full chip. Especially the energy consumption of output pads does not have to be included in the total energy consumption.

At NXP research a suitable pad ring and a matching test board are more or less available. These will be used for the test setup. Various equal supply voltages will be used for various functions within the chip. This allows for them to be measured independently.

7.2.3 Number of bits

The number of bits is selected with a sufficiently low FOM in mind. It is exploited that the FOM does not correspond to actual limitations. Early during development formula (32) was used with several values for $E_{analog,0}$ and $E_{digital,0}$ that seemed reasonable at that time. Minimum values for the FOM were calculated at eleven and fourteen bits.

Because of easier development the value of ten bits was selected. Updated calculation based on ten bits have consistently shown a FOM that is significantly lower than currently published converters. That is why there has been no reason since to change the number of bits.

7.2.4 Basic architecture and main additional techniques

The basic architecture that is used is successive approximation. This decision is motivated in paragraph 5.6. For its level creation the alternative weighted-capacitor charge redistribution architecture is used, as described in paragraph 6.3.3. Because of its favorable noise performance the comparator introduced in paragraph 6.4.2 is used.

7.2.5 References

In paragraph 4.3.1 it was decided that it is reasonable to require one or a small number of voltage references and one current reference. This ADC does not require a current reference. Furthermore it is decided that the supply voltages will directly be used as voltage references.

In paragraph 4.3.2 it was decided that it is reasonable to require an external clock signal with a frequency that is equal or similar to the conversion frequency. The SAR algorithm requires quite a lot of successive control signals, even when no DC/DC conversion technique is applied. Because the reasonability of such a faster external clock signal is doubtful it is decided that an internal mechanism should be implemented to provide the successive control signals. It is implemented in the form of a delay line.

7.2.6 Delay line implementation

For correct operation there is only a minimum value for each delay. As a result jitter, mismatch and process variations do not particularly have to be minimized. The nominal delay can be increased instead. The delay line effectively determines the maximum operating frequency. No special attention is paid to this frequency.

Several RC-based delay architectures have been considered. Development effort focuses on getting the most resistance per parasitic capacitance. If the process option of a high resistance poly resistor would have been available the chosen implementation would likely have included it.

Instead the chosen implementation consists of asymmetrical high threshold inverters. Alternating

the length of the PMOST and of the NMOST have a high value. The width of all transistors is minimum size.

The application of current mirrors and a current reference has also been considered. Very small transistors match poorly. To get even a little current matching the current mirror transistors should be biased sufficiently far in strong inversion instead of in weak inversion. Strong inversion requires a large length of the transistors because of the very small currents. The resulting solution is quite similar to the chosen implementation with asymmetrical inverters.

The most delay for a given energy consumption can be achieved at a lowered supply voltage. It is decided to use $1\,V$ as the supply voltage instead of the process default of $1.2\,V$.

7.2.7 Capacitor value and converter range

As discussed in paragraph 6.3.9 the lower limit of the hold capacitor value depends on matching. It can be calculated with formula (51). As discussed in paragraph 3.2.2 the parameter A_C can not be obtained from the design manual. The value used in formula (52) is close to the parameter A_C for fringe capacitors in the design manuals for 65 nm and 90 nm. Estimation (52) is used, yielding a capacitor value of $630\,fF$. The actual parameter A_C depends on layout and unknown process parameters. It can be obtained from measurement.

The range of a single-ended version of the DAC is rail-to-rail. As concluded in paragraph 6.4.4 a large input voltage range is favorable for the comparator energy consumption. It is decided to implement the ADC differentially, effectively doubling the range. The effective range is now $2\,V$.

A differential implementation does not influence the total value of the hold capacitance. Both halves can have half the value of the single-ended value. Absolute noise and mismatch are doubled, but so is the range.

7.2.8 Application of DC/DC conversion techniques

Both DC/DC conversion techniques discussed in paragraph 6.3.6 are considered for application. The maximum equivalent capacitor that needs to be charged or discharged is less than a quarter of the hold capacitor, at most approximately $150\,fF$. An optimistic estimation for a maximum value for an on chip inductor is $20\,nH$. A corresponding period is calculated in formula (67). The actual switching time and required accuracy are shorter. When comparing this value to the rise time of an inverter it is concluded that this DC/DC conversion technique is not suitable for this project.

$$T = 2 \cdot \pi \cdot \sqrt{L \cdot C} \approx 340[\,ps] \tag{67}$$

The step-wise DC/DC conversion technique is implemented instead and only on some of the more significant bits. Because of the supply voltage of $1\,V$ and the lack of low threshold transistors it is not possible to implement a switch that reasonably conducts at half the supply voltage under all process variations. It is decided that two intermediate steps will be used, at $1/3\,V$ and at $2/3\,V$.

As discussed in paragraph 6.3.6 the voltage sources can be implemented by large capacitors to any supply voltage. For this implementation large capacitors are split into parts and these are connected to opposite supply voltages. Their ratio is chosen such that voltage division at start up gives the initial voltage a favorable value.

7.2.9 Comparator implementation

The comparator introduced in paragraph 6.4.2 is implemented. The total capacitance as intended in formula (62) is about $20\,fF$. According to calculation the input-referred noise voltage should be in

the order of $0.5\,mV$. Simulations indicate a value that is about three times as large. The simulation is known to be inaccurate. The actual performance can only be identified through measurement. An extra comparator separate from the ADC is added to the chip to allow more testing flexibility.

7.2.10 Bootstrapped differential sample-and-hold

The requirements for the sample-and-hold circuit are that it works with a sufficiently low distortion over the full voltage range at a relatively low speed. A simple transmission gate does not meet these requirements. Low threshold transistors are not available and using standard threshold transistors its worst case conduction around half the supply voltage is too low or its charge injection too large.

A reliable single-ended bootstrapped circuit is found in literature [8]. It is straightforwardly implemented differentially and meets the requirements according to simulation. Very little optimization is done because the requirements are already met at sufficiently low power dissipation.

7.3 Post layout simulation results

The post layout simulated energy consumption is 1.9 pJ / conversion. Its various contributions are shown in figure 12. It includes a full conversion including the ADC being reset after 600 ns.

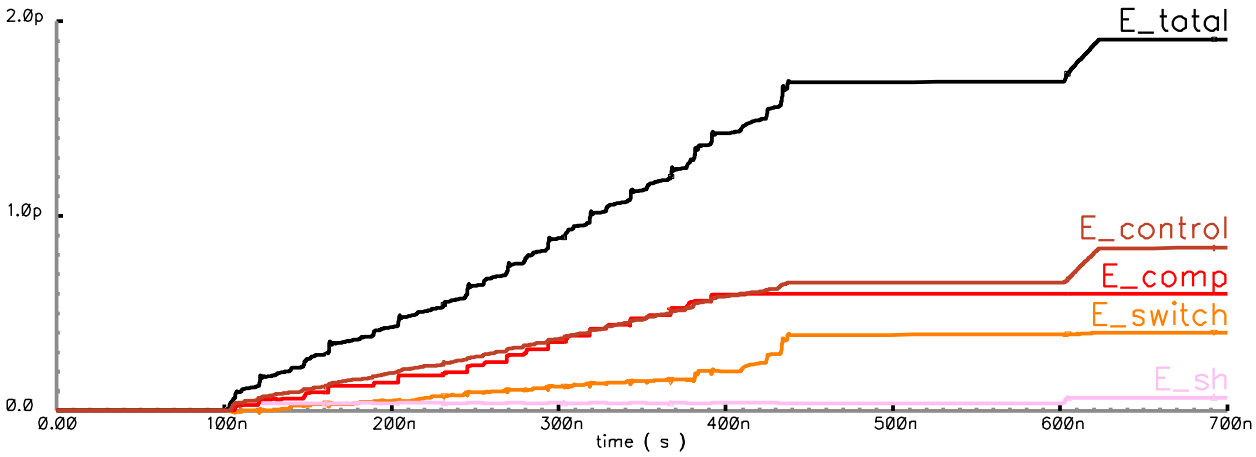

Figure 12: Energy consumption of ADC

E_control is the energy that is dissipated in the control path. It consists of the delay line and the combinational logic generating the control signals for the various stages of the SAR algorithm and the DC/DC conversion. E_comp is the energy dissipated in the comparator. E_switch is the energy dissipated by the DC/DC conversion for the level creation. It also includes the output latches. E_sh is the energy dissipated in the sample-and-hold circuit.

The actual noise performance of the comparator and the actual capacitor matching are unknown. A possible estimation is that the standard deviation of each of them is half the LSB voltage. If this is true the noise energy of each of them is three times as large as the quantization noise energy. Combined the energy is about six times as large as quantization noise energy. It can be assumed to be dominant. The SINAD is reduced by about 7.8 dB resulting in a FOM of about 4.6 fJ / conversion-step.

7.4 Future work

A final conclusion about the developed chip requires measurements. The most important measurements are on the SINAD and the energy consumption of the developed ADC. Time does not allow to perform these as part of this graduation project.

8 Conclusions and recommendations for future work

In chapter 3 limitations on low-power analog-to-digital conversion have been explored. It can be concluded that the figure of merit, a widely accepted benchmark for low-power analog-to-digital conversion, does not correspond to fundamental limitations. It can also be concluded that it depends on the number of bits how easy it is to reach a certain FOM.

In chapter 4 the scope of an ADC has been explored. It can be concluded that various conceptions exist about when a circuit deserves to be called ADC.

In chapter 5 several ADC architectures have been considered. It can be concluded that logarithmic approximation is the most suitable one for low-power analog-to-digital conversion.

In chapter 6 building blocks for low-power analog-to-digital conversion have been explored. They are mainly geared towards logarithmic approximation with the main emphasis on successive approximation. It can be concluded that application of several of these building blocks can lead to converters that are considerably more energy efficient than currently available. It can also be concluded that there is no fundamental lower limit on energy dissipation of digital-to-analog conversion.

A promising architecture is the hybrid of a sigma delta and a SAR ADC, as described in paragraph 6.2.4. Implementation will become more and more favorable as technology scales. It is recommended to further investigate this converter.

In chapter 7 the development of chip to test and demonstrate a selection of the low-power analog-to-digital conversion techniques is described. It should be measured.

9 References

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